

Claims

[c1] 1. A method for independently refreshing a memory capacitor, for a system at least comprising a refresh controller coupled to an input terminal of a pre-decoded row address counter, an output terminal of said pre-decoded row address counter being coupled to an input terminal of a pre-decoded row address re-driver, said method comprising:

 said refresh controller providing a refresh control signal;

 said pre-decoded row address counter counting a regular pre-decoded row address in response to said refresh control signal;

 inputting said regular pre-decoded row address to said pre-decoded row address re-driver to obtain a row address; and

 refreshing a memory capacitor according to said row address.

[c2] 2. The method of claim 1, further comprising

 determining one of an address counting data and an address signal according to a control signal; and

 inputting said determined one of said address counting data and said address signal to said pre-decoded row

address re-driver.

[c3] 3. An apparatus for refreshing a memory capacitor, comprising:
a refresh controller providing a refresh control signal;
a pre-decoded row address counter, said pre-decoded row address counter comprising a plurality of pre-decoded row address lines, said pre-decoded row address counter being couple to said refresh controller and receiving said refresh control signal to count, said pre-decoded row address counter outputting a regular pre-decoded row address in response to said refresh control signal via said pre-decoded row address lines;
a pre-decoded row address re-driver, coupled to said plurality of pre-decoded row address lines, for receiving and re-driving said corresponding pre-decoded row address and outputting a pre-decoded row address; and
a core device coupled to said pre-decoded row address re-driver, wherein said core device refreshes a memory capacitor according to said pre-decoded row address.

[c4] 4. The apparatus of claim 3, wherein said pre-decoded row address counter has N input terminals and has 2^N pre-decoded row address lines.

[c5] 5. The apparatus of claim 3, wherein said pre-decoded row address re-driver further comprises:

a selecting device, for selecting a signal from an input terminal of said selecting device and outputting an address signal; and

a multiplexer, coupled to said selecting device, for outputting one of said address signal and said regular pre-decoded row address according to a control signal.

[c6] 6.The apparatus of claim 5, wherein said selecting device is a NAND gate.

[c7] 7.The apparatus of claim 5, wherein said multiplexer comprises two transmission gates.

[c8] 8.The apparatus of claim 5, wherein said pre-decoded row address re-driver comprises:

a first buffer, coupled to said multiplexer and said selecting device, for receiving and stabilizing said address signal, and adjusting a transmitting rate of said address signal; and

a second buffer, coupled to said selecting device, for receiving and stabilizing said one of said address signal and said regular pre-decoded row address, and for adjusting a transmitting rate of said one of said address signal and said regular pre-decoded row address.

[c9] 9.The apparatus of claim 8, wherein said first buffer and

said second buffer are inverters.